In the Claims:

Please cancel claims 11-35 without any disclaimer and a prejudice to and add the following claims.

Listing of claims is as follows:

1. (Original) A thin film transistor array panel for a liquid crystal display, comprising:

an insulating substrate including a display area, a peripheral area at the circumference of the display area, and an outer area comprising other than the display area and the peripheral area;

a black matrix formed on the display area of the insulating substrate and having an opening of a matrix array corresponding to pixels;

red, blue and green color filters formed at the pixels on the insulating substrate;

an insulating layer covering the black matrix and the color filters;

a gate wire including a gate line and a gate electrode connected to the gate line, and formed on the insulating layer;

a gate insulating layer covering the gate wire on the insulating layer;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode that are made of a same layer on the semiconductor pattern and separated from each other, and a data line connected to the source electrode and defining a pixel in a matrix array by crossing the gate line;

a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and

a pixel wire including a pixel electrode connected to the drain electrode through the first contact hole.

2. (Original) The thin film transistor array panel of claim 2, further comprising an alignment key formed of a same layer as the black matrix or the color filters of the outer area.

3. (Original) The thin film transistor array panel of claim 1, further comprising a common wire formed of the same layer as the black matrix and including a common signal line transmitting common signal to common electrode opposing the pixel electrode and common pads transmitting the common signal to the common signal line from external circuits and connected to the common signal line.

4. (Original) The thin film transistor array panel of claim 1, wherein the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and

wherein the gate pad or the data pad are formed with the same layer as the black matrix, the gate wire, or the data wire on the peripheral area.

5. (Original) The thin film transistor array panel of claim 4, wherein the pixel wire further comprises a redundant gate pad and a redundant data pad which are made of a same layer as the pixel electrode and are respectively connected to the gate pad and the data pad through second and third contact holes of the gate insulating layer or the passivation layer.

6. (Original) The thin film transistor array panel of claim 5, wherein the gate pad and the data pad are formed with the same layer as the black matrix, and the passivation layer and the gate insulating layer have a fourth and a fifth contact hole to connect the gate pad and the data pad to the gate line and the data line, respectively.

7. (Original) The thin film transistor array panel of claim 1, wherein edges of the red, green and blue color filters overlap the black matrix.

8. (Original) The thin film transistor array panel of claim 1, wherein the insulating layer is planar and is made of organic insulating material.

9. (Original) The thin film transistor array panel of claim 1, wherein the black matrix, the gate wire, or the data wire have single-layered structure made of aluminum, aluminum alloy, copper or copper alloy, or multi-layered structure including a conductive material of chromium, molybdenum, molybdenum ally, chromium nitride or molybdenum nitride.

10. (Original) A manufacturing method of a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a black matrix on a display area of an insulating substrate including a display area, a peripheral area around the circumference of the display area, and an outer area comprising an area other than the display area and the peripheral area;

forming red, blue and green color filters on the insulating substrate;

forming an insulating layer covering the black matrix and the color filters;

forming an alignment key on the outer area.

forming a gate wire including a gate line and a gate electrode connected to the gate line on the insulating layer;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer of the gate electrode;

forming a data wire including a source electrode and a drain electrode, and a data line defining the pixels of a matrix array by crossing the gate line; and

forming a pixel electrode connected to the drain electrode.

11-35 (Cancelled)